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1 Saving the world from bad beans: deployment-time confinement checking   ▱
Dave Clarke, Michael Richmond, James Noble
October 2003 **ACM SIGPLAN Notices , Proceedings of the 18th ACM SIGPLAN conference on Object-oriented programing, systems, languages, and applications**, Volume 38 Issue 11
Full text available: 🗎 pdf(380.32 KB)   Additional Information: full citation, abstract, references, index terms

The Enterprise JavaBeans (EJB) framework requires developers to preserve architectural integrity constraints when writing EJB components. Breaking these constraints allows components to violate the transaction protocol, bypass security mechanisms, disable object persistence, and be susceptible to malicious attacks from other EJBs. We present an object confinement discipline that allows static verification of components' integrity as they are deployed into an EJB server. The confinement rules are ...

Keywords: confinement, deployment tools, enterprise JavaBeans

2 Web-based and Java-based simulation: Finding a substrate for federated components on the web   ☐
John A. Miller, Andrew F. Seila, Junxiu Tao
December 2000 **Proceedings of the 32nd conference on Winter simulation**
Full text available: 🗎 pdf(85.61 KB)   Additional Information: full citation, abstract, references

Recent developments in software component technology have renewed the promise of reusable software. Combining this with the possibilities of sharing simulation results and models using the Internet makes these new developments all the more important, particularly for Web-Based Simulation. Interoperability standards and data interchanges standards (e.g., XML) help facilitate having simulation models interact with other simulation models as well as other information technology components. This pap ...

3 MultECommerce: a distributed architecture for collaborative shopping on the WWW   ☐
Stefano Puglia, Robert Carter, Ravi Jain
October 2000 **Proceedings of the 2nd ACM conference on Electronic commerce**
Full text available: 🗎 pdf(690.44 KB)   Additional Information: full citation, references, citings, index terms

Keywords: WWW engineering, component technologies, e-commerce APIs, e-commerce

architectures, enterprise JavaBeans, shared navigation

4 Component-centric approach in a web-based home schooling application

Lin Chen, Youwen Ouyang

March 2001 **Proceedings of the 2001 ACM symposium on Applied computing**

Full text available: pdf(210.33 KB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>index terms</u>

Keywords: JSP, client/server, component-centric, education and technology transfer, web-based application

5 A principled design for scalable internet visual communications with rich media, interactivity, and structured archives

Ron Baecker

October 2003 **Proceedings of the 2003 conference of the Centre for Advanced Studies conference on Collaborative research**

Full text available: pdf(1.44 MB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

In contrast to video conferencing, webcasting supports scaleable Internet visual communications, yet it is typically viewed as an ephemeral one-way broadcast medium. We present a principled design for interactive webcasts that are accessible both in real-time and retrospectively. We derive system architecture and functionality from project goals, results from the video communications literature, and observations of prototype implementations in real webcasts. The ePresence system is scalable, int ...

6 Session 9A: System level test and reliability: Accurate CMOS bridge fault modeling with neural network-based VHDL saboteurs

Don Shaw, Dhamin Al-Khalili, Côme Rozon

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(137.79 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

This paper presents a new bridge fault model that is based on a multiple layer feedforward neural network and implemented within the framework of a VHDL saboteur cell. Empirical evidence and experimental results show that it satisfies a prescribed set of bridge fault model criteria better than existing approaches. The new model computes exact bridged node voltages and propagation delay times with due attention to surrounding circuit elements. This is significant since, with the exception of full ...

Keywords: CMOS ICs, VHDL, bridge defects, fault models, fault simulation, neural networks

7 Performance of Bluetooth bridges in scatternets with limited service scheduling

Vojislav B. Mišic´, Jelena Mišic´

February 2004 **Mobile Networks and Applications**, Volume 9 Issue 1

Full text available: pdf(552.34 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

The performance of two Bluetooth piconets linked through a bridge device is analyzed using the tools of queueing theory. We analyze both possible cases, i.e., when the bridge device is the master in one of the piconets and a slave in the other (MS bridge), as well as when the bridge device is the slave in both of the piconets (SS bridge). Analytical results are derived

for the probability distribution of access delay (i.e., the time that a packet has to wait before being serviced) and end-to-end ...

Keywords: Bluetooth, Bluetooth scatternet, master/slave bridge, performance evaluation, queueing theory, slave/slave bridge

8 A circuit level fault model for resistive bridges

Zhuo Li, Xiang Lu, Wangqi Qiu, Weiping Shi, D. M. H. Walker
October 2003 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 8 Issue 4
Full text available: pdf(183.92 KB)   Additional Information: full citation, abstract, references, index terms

Delay faults are an increasingly important test challenge. Modeling bridge faults as delay faults helps delay tests to detect more bridge faults. Traditional bridge fault models are incomplete because these models only model the logic faults or these models are not efficient to use in delay tests for large circuits. In this article, we propose a physically realistic yet economical resistive bridge fault model to model delay faults as well as logic faults. An accurate yet simple delay calculation ...

Keywords: bridge faults, delay faults, fault models

9 Detecting bridging and stuck-at faults at input and output pins of standard digital components

Mark Karpovsky, Stephen Y.H. Su
June 1980 **Proceedings of the seventeenth design automation conference on Design automation**
Full text available: pdf(904.10 KB)   Additional Information: full citation, abstract, references, citings, index terms

Due to the advances in the integrated circuit technology, there is an increasing importance in testing bridging (short circuit) failures in digital networks. Unfortunately, very little work has been done in this area. This paper presents the schemes for the detection of feedback bridgings between the inputs and outputs through the observation of oscillation and asynchronous behavior of sequential networks created by bridging faults. The lower and upper bounds on the number of tests for dete ...

10 A computer science perspective of bridge design

Alfred Spector, David Gifford
April 1986 **Communications of the ACM**, Volume 29 Issue 4
Full text available: pdf(3.51 MB)   Additional Information: full citation, abstract, references, citings, index terms

What kinds of lessons does a classical engineering discipline like bridge design have for an emerging engineering discipline like computer systems design? Case-study editors Alfred Spector and David Gifford consider the insight and experience of bridge designer Gerard Fox to find out how strong the parallels are.

11 STAR: a transparent spanning tree bridge protocol with alternate routing

King-Shan Lui, Whay Chiou Lee, Klara Nahrstedt
July 2002 **ACM SIGCOMM Computer Communication Review**, Volume 32 Issue 3
Full text available: pdf(289.47 KB)   Additional Information: full citation, abstract, references, index terms

With increasing demand for multimedia applications, local area network (LAN) technologies are rapidly being upgraded to provide support for quality of service (QoS). In a network that consists of an interconnection of multiple LANs via bridges, the QoS of a flow depends on

h   c   g e   cf   c

the length of an end-to-end forwarding path. In the IEEE 802.1D standard for bridges, a spanning tree is built among the bridges for loop-free frame forwarding. Albeit simple, this approach does not support all-pair shortest p ...

12 SmartBridge: a scalable bridge architecture

Thomas L. Rodeheffer, Chandramohan A. Thekkath, Darrell C. Anderson

August 2000 **ACM SIGCOMM Computer Communication Review , Proceedings of the conference on Applications, Technologies, Architectures, and Protocols for Computer Communication**, Volume 30 Issue 4

Full text available: ⬛ pdf(202.23 KB)   Additional Information: full citation, abstract, references, citings, index terms

As the number of hosts attached to a network increases beyond what can be connected by a single local area network (LAN), forwarding packets between hosts on different LANs becomes an issue. Two common solutions to the forwarding problem are IP routing and spanning tree bridging. IP routing scales well, but imposes the administrative burden of managing subnets and assigning addresses. Spanning tree bridging, in contrast, requires no administration, but ofte ...

13 Design and implementation of a software bridge with packet filtering and statistics collection functions

A. Khan, N. Al-Darwish, M. Guizani, M. Benten, H. Youssef

September 1997 **International Journal of Network Management**, Volume 7 Issue 5

Full text available: ⬛ pdf(255.41 KB)   Additional Information: full citation, abstract, references, index terms

This article starts with the formulation of the complete design problem. Possible design strategies are then identified and adopted along with the reasons for adoption. Finally, the article describes the implementation of the proposed bridge. © 1997 John Wiley & Sons, Ltd.

14 A deductive technique for diagnosis of bridging faults

Srikanth Venkataraman, W. Kent Fuchs

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**

Full text available: ⬛ pdf(118.76 KB)
                   ⬛ Publisher Site   Additional Information: full citation, abstract, references, index terms

A deductive technique is presented that uses voltage testing for the diagnosis of single bridging faults between two gate input or output lines and is applicable to combinational or full-scan sequential circuits. For defects in this class of faults the method is accurate by construction while making no assumptions about the logic-level wired-AND/OR behavior. A path-trace procedure starting from failing outputs deduces potential lines associated with the bridge and eliminates certain faults. The ...

Keywords: Bridging faults, Diagnosis, Deduction.

15 Active bridging

D. Scott Alexander, Marianne Shaw, Scott M. Nettles, Jonathan M. Smith

October 1997 **ACM SIGCOMM Computer Communication Review , Proceedings of the ACM SIGCOMM '97 conference on Applications, technologies, architectures, and protocols for computer communication**, Volume 27 Issue 4

Full text available: ⬛ pdf(1.73 MB)   Additional Information: full citation, abstract, references, citings, index terms

Active networks accelerate network evolution by permitting the network infrastructure to be

programmable, on a per-user, per-packet, or other basis. This programmability must be balanced against the safety and security needs inherent in shared resources.This paper describes the design, implementation, and performance of a new type of network element, an Active Bridge. The active bridge can be reprogrammed "on the fly", with loadable modules called switchlets. To demonstrate the use of the active ...

16 Diagnosis of realistic bridging faults with single stuck-at information

Brian Chess, David B. Lavo, F. Joel Ferguson, Tracy Larrabee

December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(158.82 KB)   Additional Information: full citation, abstract, references, citings, index terms
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Abstract: Precise failure analysis requires accurate fault diagnosis. A previously proposed method for diagnosing bridging faults using single stuck-at dictionaries was applied only to small circuits, produced large and imprecise diagnoses, and did not take into account the Byzantine Generals Problem for bridging faults. We analyze the original technique and improve it by introducing the concepts of match restriction, match requirement, and failure recovery. Our new technique, which requires no ...

Keywords: failure analysis, failure recovery, fault diagnosis, fault location, logic testing, match requirement, match restriction, realistic bridging faults diagnosis, single stuck-at dictionaries, single stuck-at information, stuck-at diagnosis, stuck-at methods

17 Bridge fault simulation strategies for CMOS integrated circuits

Brian Chess, Tracy Larrabee

July 1993 **Proceedings of the 30th international on Design automation conference**

Full text available: pdf(568.33 KB) Additional Information: full citation, references, citings, index terms

18 A high performance transparent bridge

Martina Zitterbart, Ahmed N. Tantawy, Dimitrios N. Serpanos

August 1994 **IEEE/ACM Transactions on Networking (TON)**, Volume 2 Issue 4

Full text available: pdf(1.41 MB)   Additional Information: full citation, references, index terms

19 BIFEST: a built-in intermediate fault effect sensing and test generation system for CMOS bridging faults

Kuen-Jong Lee, Jing-Jou Tang, Tsung-Chu Huang

April 1999 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 4 Issue 2

Full text available: pdf(208.73 KB)   Additional Information: full citation, abstract, references, index terms

This paper presents BIFEST, an ATPG system that employs the built-in intermediate voltage test technique in an efficient ATPG process to deal with CMOS bridging faults. Fast and accurate calculations of the intermediate bridging voltages and the variant threshold tolerance margins on a resistive bridging fault model are presented. A PODEM-like, PPSFP-based ATPG process is developed to generate test patterns for faults that are conventionally logic-testable. The remaining faults are then dea ...

20 GOLDENGATE: a fast and accurate bridging fault simulator under a hybrid logic/IDDQ testing environment

Tzuhao Chen, Ibrahim N. Hajj

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(169.23 KB)

Publisher Site

Additional Information: full citation, abstract, references, index terms

In this paper we describe GOLDENGATE-a bridging fault simulator for cell-based digital VLSI circuits with the following features: 1. It targets both combinational and sequential circuits. 2. It simulates general (routing, adjacency, and intra-cell) realistic bridging faults efficiently through a table-based scheme. The pre-computed table contains accurate cell output voltage and I/sub DDQ/ values obtained through electrical-level simulations. 3. It simulates both feedback and nonfeedback bridgin ...

Keywords: GOLDENGATE, bridging fault simulator, combinational circuits, digital VLSI circuits, electrical-level simulation, event-driven technique, logic testing, logic/I/sub DDQ/ testing, sequential circuits

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